Specification Amendments

Please replace paragraph 004 with the following rewritten paragraph:

004 For example, the presence of a relatively rough surface due to the penetration of pore openings at the surface of an opening etched into a low-K IMD layer produces surface micro-openings adversely affecting coverage of overlying deposited layers, for example diffusion barrier layers and seed layers. As a result, thicker barrier layers, with increased series resistance are required in order to avoid forming barrier layers having pinholes which undesirably allow electromigration of metal into the IMD layer. Further, the deposition of seed layers, typically formed by PVD processes, may be non-continuously formed, thereby adversely affecting electro-chemical deposition processes. For example, non-contiguous seed layers, for example, including as pin holes, can cause the formation of voids within the copper filling portion of an ECP deposited copper layer.

Please replace paragraph 0013 with the following rewritten paragraph:

0013 Although the present invention is explained by reference to an exemplary dual damascene formation process, it will be appreciated that the method of the present invention applies generally to the formation of damascenes including single vias and trench lines extending through single or multiple IMD layers. While the method is particularly advantageous for forming copper damascenes in porous low-K dielectrics, it will be appreciated that the method may be applied to the formation of other metal damascenes and other dielectric insulating layers, particularly where damascene opening aspect ratios are greater than about 4, where the method of the present invention will advantageously improve step coverage of seed layers to improve a copper ECP process.

Please replace paragraph 0016 with the following rewritten paragraph:

0016 Referring to Figure 1A, a substrate including for example metal interconnect portion 11, is formed in a dielectric insulating layer 10 by conventional processes known in the micro-electronic integrated circuit manufacturing ~~process~~ art followed by deposition of an overlying first etching stop layer 12, for example, silicon nitride (e.g., SiN, Si_3N_4) or silicon carbide

(e.g., SiC) to a thickness of about 300 Angstroms to about 700 Angstroms by conventional CVD processes, for example, LPCVD or PECVD.

Please replace paragraph 0017 with the following rewritten paragraph:

0017 Still referring to Figure 1A, formed over first etching stop layer 12 is dielectric insulating layer 14, for example an inter-metal dielectric (IMD) layer, preferably formed of a low-K dielectric material, for example a silicon oxide based material having a porous structure. By the term 'low-K dielectric' is meant having a dielectric constant less than about 3.0, preferably less than about 2.7. The dielectric insulating layer portion 14, in one embodiment is preferably formed by a CVD process, for example LPCVD or PECVD including organo-silane precursors such methylsilanes, including tetramethylsilane and trimethylsilane. In addition, organo-siloxane precursors such as cyclo-tetra-siloxanes such as tetramethylcyclotetrasiloxane, octamethylcyclotetrasiloxane, and decamethylcyclopentasiloxane may be suitably used to form the IMD layer portion 14[[A]]. It will be appreciated that inorganic or organic spin-on glasses (SOG) may also be used, for example including organo-silane or

organo-siloxane precursors which are spun on the substrate by conventional methods followed by a curing process including optional post curing thermal and plasma treatments.

Please replace paragraph 0022 with the following rewritten paragraph and delete paragraph 0023 as follows:

0022 Referring to Figure 1D, in an important aspect of the invention, a first seed layer 22 is deposited on the diffusion barrier layer to a thickness of about 50 Angstroms to about 300 Angstroms. In one embodiment, the first seed layer 22 is deposited to form a substantially non-conformal layer. The term 'substantially non-conformal' means that the sidewalls and/or bottom portion of the opening receive less than about 10% of the deposited coverage (thickness) compared to the substrate process surface. To deposit the substantially non-conformal seed layer, a PVD process is preferred. In another embodiment, the first seed layer 22 is deposited (e.g., blanket deposited) to form a substantially conformal layer. The term 'substantially conformal' means that the sidewalls and/or bottom portion of the opening receive greater than about 10% of the deposited coverage (thickness) compared to the substrate process surface. To deposit the substantially conformal seed layer, one of a CVD,

IMP, SIP, and electroless process is preferred. Preferably the first seed layer 22 is formed of one of Cu, Ti, TiN, Ta, TaN, Cr, CrN, W, and WN. In a preferred embodiment, the ~~second~~ first seed layer is copper. It will be appreciated that the metal nitrides as listed are intended to include other stoichiometries of both metal and nitrogen different from 1 including e.g., TiNx, TaNx, CrNx, where x is different from 1, e.g., greater than 1.

0023 ~~metal and nitrogen different from 1 including e.g., TiNx, TaNx, CrNx, where x is different from 1, e.g., greater than 1.~~

Please replace paragraph 0028 with the following rewritten paragraph:

0028 Following deposition of the second seed layer 24, a second plasma treatment process is carried out according to the same preferred embodiments for the first seed layer 22 plasma treatment process, but may include [[a]] different or the same plasma source gases, e.g., Ar, N_2, NH_3, or N_2/H_2. Preferably, the second seed layer plasma treatment is carried out in-situ with respect to the deposition of the second seed layer for the same reasons outlined for preferably carrying out the first seed layer plasma treatment in-situ, and is preferably formed substantially

oxide-free.

Please replace paragraph 0030 with the following rewritten paragraph:

0030 Thus, a method and copper damascene structure has been presented including the forming of a multi-layer seed layer has advantageously providing for improved seed layer step coverage of high aspect ratio openings, for example greater than about 4:1 including greater than about 6:1. Furthermore, the method of the present invention is particularly advantageously applied to damascenes including a critical dimension of less than about 0.13 microns, for example including 65 nm and 90 nm critical dimensions. Advantageously, by ensuring formation of a continuous seed layer in high aspect ratio openings, the formation of defects in the ECP process, including voids, are avoided thereby improving the performance and reliability of ECP of copper damascenes. By providing for seed layer plasma treatment processes according to preferred embodiments, the presence of oxides on the seed layer surface is avoided, thereby further avoiding defect formation in the copper ECP process such as voids and further improving the electrical performance and reliability of copper damascenes.

Please replace paragraph 0031 with the following rewritten paragraph:

0031 Referring to Figure 2 is shown a process flow diagram including several embodiments of the present invention. In process 201, a semiconductor substrate including underlying metal interconnects is provided. In process ~~202~~ 203, a low-K IMD layer is formed. In process 205, a damascene opening is formed in the IMD layer. In process 207, a diffusion barrier layer is blanket deposited to line the dual damascene opening according to preferred embodiments. In process 209, a first seed layer is formed according to preferred embodiments over the diffusion barrier layer. In process 211, a first plasma treatment of the first seed layer is carried out according to preferred embodiments. In process 213 a second seed layer is formed according to preferred embodiments over the first seed layer. In process 215, a second plasma treatment of the second seed layer is carried out according to preferred embodiments. In process 217 the damascene is filled with copper by a copper ECP process. In process 219, a planarization process is carried out to form copper filled damascene.